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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,417	08/24/2001	Leonard Forbes	MICRON.154A / 00-0184	4204

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EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/939,417	FORBES, LEONARD
	Examiner	Art Unit
	Monica Lewis	2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2002*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This office action is in response to the amendment filed August 24, 2002.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Forbes et al. (U.S. Patent No. 5,936,274).

In regards to claims 1 and 20, Forbes et al. discloses (Col. 1; line 50 to 55) a memory cell includes a pillar 300 of semiconductor material that extends outwardly from a working surface of a substrate. (Col. 1; line 50 to 55). The floating gate transistor includes a first conductivity type semiconductor pillar. (Col. 1; line 64 to 67). The floating gate transistor 105 and 200 includes a first conductivity type semiconductor pillar. The pillar has top and side surfaces and is formed upon the substrate. (Col. 2; line 1 to 5). A first source/drain region, of a second conductivity type, is formed proximal to an interface between the pillar and the substrate. A second source/drain region, of a second conductivity type, is formed in a portion of the pillar that is distal to the substrate and separate from the first source/drain region. (Col. 2; line 19 to 25). A second source/drain region, of a second conductivity type, is formed in a portion of the pillar that is distal to the substrate and separate from the first source/drain region. A gate dielectric 330 and 1000 is formed on at least a portion of the side surface of the pillar. (Col. 2; line 29 to 31).

An intergate dielectric 340 and 1300 is formed, interposed between each of the substantially adjacent floating and control gates (Col. 7; line 1 to 4). Cells 205 has two floating gate transistors 200, such as cell 205BB. In FIG. 4, each of the two floating gates 325 is adjacent to one of opposing sides of pillar 300, and separated therefrom by gate dielectric 330. (Col. 7; line 4 to 10) Each control gate 335 is separated from a corresponding floating gate 325 by an intergate dielectric 340. Each control gate 335 is integrally formed together with one of the gate.

Regarding claims 2, 4, 7, 8, 18,19, 21 and 22, (Col. 3; line 30 to 35) each control gate is associated with a floating gate so as to allow programming by selective storage and retrieval of data on the floating gates (Col. 8; line 15 to 20) if there are no electrons stored on the floating gate 325, the floating gate transistor 200 will conduct between its source region 310 and drain region 315. (Col. 8; line 21 to 25). If there are electrons stored on the floating gate 325, the floating gate transistor 200 will not conduct between its source region 310 and drain region 315. (Col. 7; line 28 to 30). Programming of one of the floating gate transistors 200 is by hot electron injection. (Col. 7; line 55 to 57) The floating gate transistor 200 may be programmed instead by Fowler-Nordheim tunneling of electrons (Col. 3; line 30 to 35). If a floating gate transistor is used to store a single bit of data, an area of only 2F.sup.2 is needed per bit of data.

Regarding claims 3 and 10, (Col. 10, line 45 to 60) a selective etch, which preferentially removes silicon dioxide but doesn't substantially remove polysilicon, is used to etch into portions of silicon dioxide insulator 605, but not the portions of polysilicon conductive layer 1005 in second troughs 700. (Col. 11; line 28 to 31) An isotropic chemical etch is used to fully undercut the semiconductor regions or pillar separating the first troughs 600, and a subsequent oxidation step is used to fill in the evacuated regions formed by the undercutting.

Regarding claims 5, 6 and 11, (Col. 5; line 34 to 40) In one embodiment, substrate 305 is a bulk semiconductor, such as P- silicon. In another embodiment, a semiconductor-on-insulator (SOI) substrate 305 includes an insulating layer, such as silicon dioxide Si02. (Col. 5; line l to 5) A number of vertical floating gate (extend outwardly) field-effect transistors (FETS) formed on the sides of a semiconductor pillar on a substrate.

Regarding claims 9 and 13, (ABSTRACT) First source/drain terminals are row addressable, which is arranged in rows. Second source/drain terminals are column addressable, which is arranged in columns. (Col. 2; line 5 to 10) a gate dielectric 330 is formed on at least a portion of the side surface of the pillar. A plurality of floating gates are formed on opposing sides of the pillar 300. Each floating gate 325 is substantially adjacent to a portion of the side surface of the pillar and separated therefrom by the gate dielectric. A plurality of control gates are formed, each of which is substantially adjacent to one of the floating gates and insulated therefrom. An intergate dielectric 340 is formed, interposed between each of the substantially adjacent floating and control gates.

Regarding claims 12 and 14, (Col. 6; line 15 to 25) each floating gate 325 has a corresponding substantially adjacent control gate 335, from which it is separated by an intergate dielectric 340. Except at the periphery of array 105, each control gate 335 is interposed between two approximately adjacent pillars 300 and shared by two floating gate transistors 200, each of these floating gate transistors 200 having portions in one of the two approximately adjacent pillars 300.

Regarding claims 15, 16 and 17, (Col. 6; line 33 to 36) (FIG. 1) each of the gate lines XG1, XG2, XGN interconnects along the column ones of the control gates 335. For example, gate line XG2 electrically interconnects control gates 335 (Col. 6; line 60 to 65) FIG. 3B illustrates a row of cells 205, 205AA, 205BA, 205NA, having source regions 310 electrically interconnected by one of first source/drain interconnection lines YS1, YS2, YSN, e.g. first source/drain interconnection line YS1, formed in substrate 305. (ABSTRACT) Second source/drain terminals are electrically connected or column addressable by data lines. (Col. 5; line 55 to 60) First source/drain region interconnection line YS1 electrically interconnects the source region 310 of each pillar 300 of cells 205AA, 205BA, 205NA. In one embodiment, the first source/drain interconnection lines YS1, YS2, YSN.

Response to Arguments

4. Applicant's arguments filed August 13, 2002 have been fully considered but they are not persuasive. Applicant argues that "Forbes does not teach a floating gate transistor wherein a control gate overlays a floating gate." However, Forbes does teach a control gate (335) that overlays a floating gate (325) (See Figure 4). Therefore, Applicant's arguments are not persuasive.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
October 25, 2002

AMIR ZARABIAN
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